IN THE CLAIMS

1. (Currently amended) A method for managing multiple memory devices over a range of logical memory addresses, the method comprising:

   receiving a command comprising a first logical memory address from the range of logical memory addresses;

   accessing a look-up table having logical memory addresses with their corresponding physical memory addresses from one of the plurality of ranges of physical memory addresses to find a first physical memory address, from a range of physical memory addresses, that corresponds to the first logical memory address; and

   generating a chip select signal in response to the first physical memory address;

   wherein the plurality of ranges of physical memory addresses include non-contiguous physical memory address space.

2. (Currently amended) The method of claim 1 wherein the range of physical memory addresses is contiguous.

3. (Currently amended) The method of claim 1 wherein the range of physical memory addresses is substantially equivalent to the range of logical memory addresses.

4. (Original) The method of claim 1 wherein the multiple memory devices are flash RAM devices.

5. (Currently amended) The method of claim 1 wherein the range of logical memory addresses are contiguous and the corresponding range of physical memory addresses is non-contiguous and comprised of a plurality of physical memory address sub-ranges.

6. (Currently amended) The method of claim 5 wherein a chip select signal is generated for each physical memory address sub-range.

7. (Currently amended) A method for managing multiple flash memory devices over a range of logical memory addresses, the method comprising:

receiving a command comprising a first logical memory address from the range of logical memory addresses;

accessing a look-up table having logical memory addresses with their corresponding physical memory addresses from one of the plurality of ranges of physical memory addresses to find a first physical memory address, from a range of non-contiguous physical memory addresses, that corresponds to the first logical memory address; and

generating a chip select signal in response to the first physical memory address.

8. (Currently amended) The method of claim 7 wherein receiving the command comprises a controller circuit executing an application in which the first logical memory address is read from memory along with the command.

9. (Currently amended) The method of claim 7 wherein receiving the command comprises a device manager receiving the first logical memory address from a controller circuit.

10. (Currently amended) The method of claim 9 wherein the device manager generates the chip select signal in response to the first physical memory address.

11. (Currently amended) A method for managing multiple flash memory devices over a range of logical memory addresses, the method comprising:

a controller circuit executing an application;

the controller circuit receiving a first logical memory address from the range of logical memory addresses in response to the execution of the application;

accessing a look-up table having logical memory addresses with their corresponding physical memory addresses from one of the plurality of ranges of physical memory addresses to find a first physical memory address, from a range of physical memory addresses comprising a

plurality of non-contiguous sub-ranges, that corresponds to the first logical memory address;

outputting the first physical memory address to chip select generation circuitry; and

the chip select generation circuitry generating a chip select signal in response to the first physical memory address.

12. (Currently amended) The method of claim 11 wherein each of the plurality of non-contiguous sub-ranges is substantially equal to a logical memory address range of a flash memory device of the multiple flash memory devices.

13. (Currently amended) An electronic system having a logical memory address map comprising a flash memory logical memory address range for a designed memory device, the system comprising:

a plurality of flash memory devices having a combined physical memory address range substantially equivalent to the flash memory logical memory address range;

a controller circuit coupled to the plurality of memory devices, the controller circuit adapted to access a look-up table stored in memory and comprising a plurality of logical memory addresses with their corresponding physical memory addresses to find a first physical memory address from the combined physical memory address range, comprising a non-contiguous physical memory address space, in response to a first logical memory address received from an executing software application; and

a chip select generation circuit coupled to the controller circuit and the plurality of memory devices, the chip select generation circuit transmitting a chip select signal to one of the plurality of memory devices in response to the first physical memory address.

14. (Original) The system of claim 13 wherein the controller circuit is coupled to the plurality of flash memory devices through a plurality of address lines.

15. (Canceled)

16. (Currently amended) The system of claim 13 wherein the controller circuit generates the first physical memory address in response to adding an address offset to the first logical memory address.

17. (Currently amended) An electronic system having a logical memory address map stored in memory comprising a flash memory logical memory address range for a designed memory device with corresponding physical memory addresses, the system comprising:

a processor that executes a software application, thereby generating a first logical memory address;

a plurality of flash memory devices having a combined physical memory address range, comprising a non-contiguous physical memory address space, substantially equivalent to the flash memory logical memory address range, the plurality of flash memory devices coupled to the processor over address lines; and

a device manager coupled to the plurality of flash memory devices and the processor, the device manager comprising:

a controller function adapted to access the logical memory address map and find a first physical memory address from the combined physical memory address range that corresponds to the first logical memory address; and

a chip select generation function capable of transmitting a chip select signal to one of the plurality of memory devices in response to the first physical memory address.

18. (Canceled)

19. (Currently amended) The electronic system of claim 17 wherein the controller function adds an address offset to the logical memory address to generate the physical memory address.

20. (Currently amended) In an electronic system that is controlled by a processor, a method for managing multiple flash memory devices over a range of logical memory addresses, the method comprising:

the processor executing a software application;

the processor receiving a first logical memory address from the range of logical memory addresses in response to the execution of the application;

the processor accessing a stored look-up table comprising the range of logical memory addresses with corresponding physical memory addresses to find a first physical memory address, from a range of physical memory addresses comprising a plurality of non-contiguous address sub-ranges, that corresponds to the first logical memory address;

the processor outputting the first physical memory address to chip select generation circuitry; and

the chip select generation circuitry transmitting a chip select signal, generated in response to the first physical memory address, to a first flash memory device of the multiple flash memory devices.